Dr. S. M. Rezaul Hasan

CONTACT PARTICULARS

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NEW ZEALAND

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AREAS OF EXPERTISE AND PROFESSIONAL INTEREST

ANALOGUE ELECTRONIC CIRCUITS, DIGITAL ELECTRONIC CIRCUITS, DIGITAL SYSTEMS, MICROELECTRONICS, CMOS ANALOGUE, DIGITAL, MIXED SIGNAL, RADIO FREQUENCY AND PHOTONIC/OPTICAL INTEGRATED CIRCUIT DESIGN, COMPUTER ARCHITECTURE, VLSI SYSTEM DESIGN, VLSI ARCHITECTURE, BIG DATA (RADIO ASTRONOMICAL) VLSI HARDWARE DESIGN, VLSI MICROPROCESSOR AND MICROCONTROLLER DESIGN, COMPUTER SYSTEM DESIGN, EMBEDDED CIRCUITS AND SYSTEMS, SEMICONDUCTOR DEVICES, BIO-ELECTRONICS, BIOLOGICAL (*gene-protein*) CIRCUIT DESIGN, COMMUNICATION AND SIGNAL PROCESSING CIRCUITS, POWER ELECTRONICS, CMOS POWER MANAGEMENT INTEGRATED CIRCUITS, POWER SEMICONDUCTOR DEVICES, LOW-POWER CMOS VLSI AND FPGA DESIGN, NANOELECTRONIC CIRCUITS, CMOS INTEGRTATED MICRO/NANO MECHATRONIC SYSTEMS, CMOS MEMS/NEMS AND NANO-BIO SENSORS, MICRO-PROGRAMMING, Si-Ge, GaN, GaAs, BiCMOS, COMPOUND SEMICONDUCTOR, GRAPHENE, CARBON-NANOTUBE, AND PLASTIC (ORGANIC) BASED MOS CIRCUITS.

EDUCATION:

1985 UNIVERSITY OF CALIFORNIA LOS ANGELES (UCLA), CALIFORNIA, USA.
DEPARTMENT OF ELECTRICAL ENGINEERING
DOCTOR OF PHILOSOPHY IN ELECTRICAL ENGINEERING
Ph.D. Dissertation: Distributed VLSI Image Processors and Master Quad-Slice Transformers.

1981 STATE UNIVERSITY OF NEW YORK AT BUFFALO, NEW YORK, USA.
DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING
MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

1980 BANGLADESH UNIVERSITY OF ENGINEERING & TECHNOLOGY, DHAKA, BANGLADESH.
DEPARTMENT OF ELECTRICAL ENGINEERING
BACHELOR OF SCIENCE IN ELECTRICAL ENGINEERING
Stood first in first class in graduating class.

WORK EXPERIENCE (Academic Teaching and Research):

7/2004- present MASSEY UNIVERSITY, AUCKLAND, NEW ZEALAND
TENURED RESEARCH STREAM SENIOR LECTURER RANGE 2 IN ELECTRICAL AND COMPUTER ENGINEERING (EQUIVALENT TO ASSOCIATE PROFESSOR):
Teaching & Research in Analogue Electronics, Digital Electronic Systems, Communication systems, Analogue and Mixed Signal Integrated Circuit Design, Advanced Computer Engineering, VLSI Microchip Design, RF IC Design, Bio-electronics, Developing IC Design/VLSI Design/CMOS Micro-mechatronics program & Laboratory.

1/2006- present MASSEY UNIVERSITY, AUCKLAND, NEW ZEALAND
DIRECTOR, CENTER FOR RESEARCH in ANALOGUE & VLSI MICROSYSTEM DESIGN (**CRAVE**):
Development of Research Center of Excellence in Integrated Circuit Design/VLSI System Design, RF Integrated Circuits, digital VLSI design, MEMS, IC Sensors, Big data hardware design for Astronomical signal processing (e.g., SQUARE KILOMETER ARRAY), CMOS Micro-mechatronics and VLSI Bioelectronics.

9/2000- 6/2004 UNIVERSITY OF SHARJAH, UNIVERSITY CITY, SHARJAH, U.A.E.
DEPARTMENT OF ELECTRICAL/ELECTRONICS & COMPUTER ENGINEERING
ASSOCIATE PROFESSOR OF COMPUTER ENGINEERING:
Teaching & Research in Analogue Electronics, Digital Integrated Circuit Design, VLSI Design & computer engineering. Developing IC Design/VLSI Design program & Laboratory, Undergraduate & graduate curriculum development.
Courses taught: Analogue electronics, analog CMOS IC design, digital CMOS IC design, power electronics, opto-electronics, VLSI design, digital logic design, communication electronics.

3/92 – 8/2000 UNIVERSITI SAINS MALAYSIA, MALAYSIA.
SCHOOL OF ELECTRICAL & ELECTRONICS ENGINEERING
LECTURER (3/92-3/99) AND THEN ASSOCIATE PROFESSOR(3/99-8/00) OF MICROELECTRONICS ENGINEERING & CO-CORDINATOR ANALOG & VLSI RESEARCH LABORATORY:
Set-up and developed the Analogue & VLSI Research Laboratory. Lead the research activity in the Analogue & VLSI Research Laboratory.
Courses taught: C programming, analogue CMOS IC design, RF CMOS integrated circuit design, digital CMOS IC design, CMOS VLSI design,

digital system design, computer architecture, physics of semiconductor devices, CMOS & BiCMOS process technology.

2/90 – 2/92 CURTIN UNIVERSITY OF TECHNOLOGY, BENTLEY, WESTERN AUSTRALIA.
SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING
LECTURER IN COMPUTER & ELECTRONICS ENGG.

3/86 – 12/88 NANYANG TECHNOLOGICAL UNIVERSITY, SINGAPORE
SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING
LECTURER, DEPARTMENT OF ELECTRONIC ENGINEERING

9/85 – 2/86 UNIVERSITY OF CALIFORNIA LOS ANGELES (UCLA), USA
ELECTRICAL ENGINEERING DEPARTMENT
VISITING LECTURER IN ELECTRICAL ENGINEERING:
Supervision of high frequency hybrid circuits laboratory.

9/79 – 5/80 STATE UNIVERSITY OF NEW YORK AT BUFFALO, NEW YORK, USA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
TEACHING ASSISTANT

WORK EXPERIENCE (Industrial):

2009 BLUELAB CORPORATION, TAURANGA, NEW ZEALAND
Consultant for analogue electronic pH, conductivity and temperature meters.

2001 –2002 VALENCE SEMICONDUCTOR INC., IRVINE, CALIFORNIA, USA
DUBAI DESIGN CENTER, DUBAI INTERNET CITY, DUBAI, UAE

CONSULTANT ANALOGUE MICROCHIP
DESIGN GROUP

Sigma-delta A-to-D & D-to-A design, mixed signal IC design, substrate noise analysis, high performance offset cancelled comparator design.

1995 MALAYSIA CENTER FOR ROBOTICS & INDUSTRIAL AUTOMATION

ROBOT MICROCONTROLLER DESIGN CONSULTANT
Project: Design of multi-axis digital VLSI micro-controllers for robotics & industrial automation.

1993 – 1994 ADVANCED MICRO DEVICES, PENANG, MALAYSIA

CONSULTANT
Project: Running an in-house industrial electronics course.

1987-1988 APPLIED RESEARCH CORPORATION, SINGAPORE
CONSULTANT

Duties: Lecturing on analogue & digital VLSI design to staff from various Singapore electronics companies.

6/83 - 2/86 XEROX CORPORATION ELECTRONICS DIVISION, CALIFORNIA, USA
SENIOR MEMBER, VLSI DESIGN ENGINEERING STAFF

Duties include: VLSI micro-processor architecture design, CMOS digital logic & circuit design, functional simulation, layout & logic verification, development of high speed VLSI architecture for digital document & image processing.
Project completed:
Design, fabrication & testing of a CMOS VLSI micro-processor for xerox's star workstation.

WORK EXPERIENCE (Academic Administration):

1993 Academic Panel Advisor, Institute of telecommunication and information technology, Malaysia.

2000 - 2004 Member, college research committee, college of engineering, University of Sharjah, Sharjah, UAE.

2002 - 2003 Participated in ABET accreditation of Engineering Programs, college of engineering, University of Sharjah, Sharjah, UAE.

2006 – 2010 Member, Technology & Engineering Program Committee, Massey University, New Zealand.

2015 - Paper coordinator for 281.786 : Advanced Micro and Nano Electronics
2015 - Paper coordinator for 281.785 : Advanced Computer Engineering
2004 – 2014 Paper coordinator for 281.457: Advanced Micro Technologies
2006 – 2010 Paper coordinator for 124.251: Analogue Electronics
2007- 2010 Paper coordinator for 140.271: Analogue Electronic Devices & Circuits
2009 Paper coordinator for 124.252: Digital Electronics
2013 Member EICS Equipment sub-committee
2011-2014 Development of the new redesigned BE curriculum at Massey University (contributed to the paper development for 2nd year, 3rd year and 4th year)
2012-1013, 2017 SEAT EICS Albany Seminar Co-ordinator

TEACHING INNOVATIONS:

2012-2017 (1) Development of *innovative STREAM sites* in Analogue & Digital Electronics as well as Microelectronics to enhance student learning.
(2) Development of new *active teaching and learning technique* to *substantially* enhance student learning and performance in electronics.

2020 (3) Developed **study-from-home learning materials (superior to textbook) for fully online teaching** of 281.281: Analog electronic systems, and, 281.786: Advanced Micro and Nano-electronics

2008 *Nominated Lecturer of the Year for 2008*
2013 *Nominated Lecturer of the Year for 2013*
2014 *Nominated Lecturer of the Year for 2014*
2015 *Nominated Lecturer of the Year for 2015*
2016 *Nominated Lecturer of the Year for 2016*
2017 *Nominated Lecturer of the Year for 2017*
2019 *Nominated Lecturer of the Year for 2019*

RESEARCH GRANTS, FUNDINGS, SUPPORT, SUBSIDIES & CORPORATE CONTRIBUTIONS OBTAINED:

1993 US$ 5,000
UNIVERSIT SAINS MALAYSIA SHORT-TERM RESEARCH GRANT
PROJECT: IMPLEMENTATION OF VLSI SIGNAL PROCESSING ON SINGLE CHIP SILICON

1996 US$ 62,000
MINISTRY OF SCIENCE, MALAYSIA, IRPA GRANTS
PROJECT: NOVEL LOW POWER BICMOS VLSI CIRCUIT TECHNIQUES

1997 US$ 80,000
HELPED IN SECURING FUNDING FOR WORKSTATIONS FOR IC/VLSI RESEARCH FROM INTEL PENANG, MALAYSIA

1998 US$ 2,600,000
HELPED IN SECURING FUNDING FOR LAB. EQUIPMENT & SOFTWARE DONATION FROM HP, PENANG, MALAYSIA

1999 US$ 26,000
RECIPIENT OF 1999 INTEL RESEARCH GRANT FOR THE DEVELOPMENT OF DATA ENCRYPTION VLSI MICROCHIP

2000 US$ 50,000
MINISTRY OF SCIENCE, MALAYSIA, IRPA GRANTS
PROJECT: DEVELOPMENT, DESIGN & FABRICATION OF SIGMA-DELTA A-TO-D CONVERTERS

2001 AED 30,000
RECEIVED SEED RESEARCH GRANT FROM UNIVERSITY OF SHARJAH FOR THE PROJECT: HIGH-PERFORMANCE CMOS INTEGRATED CIRCUIT AMPLIFIER DESIGN FOR OPTICAL TRANSCEIVERS IN OPTICAL NETWORKING APPLICATIONS

2005 NZ$2000
MASSEY UNIVERSITY RESEARCH FUND

PROJECT: AMPLIFIER AND FILTER DESIGN FOR NANOMETRIC CMOS RADIO INTEGRATED CIRCUITS

NZ$7000
DVC OFFICE MASSEY UNIVERSITY, ALBANY, AUCKLAND
PROJECT: STARTUP BUDGET FOR CENTER FOR RESEARCH IN ANALOG & VLSI MICROSYSTEM DESIGN (CRAVE)

NZ$14,000
IIMS RESEARCH FUND
PROJECT: SOFTWARE PROCUREMENT FOR IC/VLSI DESIGN

2006 FABRICATION SUPPORT (US$35,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 0.18μm 1.5SQ. MM. CMOS MICRO-CHIP USING THE TSMC CMOS FOUNDRY, Project Title "*Design of Novel CMOS Low Noise Pre-Amplifier for Ultra-Wideband Transceivers* "

2006 NZ$115,000
MASSEY UNIVERSITY CAPITAL EQUIPMENT FUND
PROJECT: AGILENT TEST EQUIPMENT FOR FABRICATED ANALOG & RF MICROCHIPS

2007 FABRICATION SUPPORT (US$50,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 5SQ. MM. CMOS MICRO-CHIP USING THE IBM CMOS FOUNDRY, Project Title "*Multi-Path Interference Cancelling FM Demodulator Using Composite Amplitude Locked loop and PLL* "

NZ$6,000
MASSEY UNIVERSITY RESEARCH FUND (MURF)
ULTRAWIDEBAND TRANSCEIVER MICROCHIP DESIGN IN 0.13μm CMOS

2007 NZ$ 8000
ITE MINOR CAPITAL FUND
PROJECT: S-PARAMETER MEASUREMENT MODULE

2009 NZ$110,000
MASSEY UNIVERSITY CAPITAL EQUIPMENT FUND
PROJECT: MICROPROBING FABRICATED ANALOG, RF AND BIO MICROCHIPS

2009 FABRICATION SUPPORT (US$50,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 4.6SQ. MM. CMOS MICRO-CHIP USING THE IBM CMOS FOUNDRY, Project Title "*Development of Single-Chip Temperature Sensor and Associated Analogue and Data-Conversion Circuit* "

2010 FABRICATION SUPPORT (US$100,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 9 SQ. MM. CMOS MICRO-CHIP USING THE IBM CMOS FOUNDRY, Project Title "*Design of a Novel CMOS RF Front-end for Ultra-Wide-Band Receiver*"

2011 NZ$ 16,000
MASSEY UNIVERSITY RESEARCH FUND (MURF)
CMOS RF RESONATOR BASED MEMS PRESSURE SENSOR

2012 FABRICATION SUPPORT (US$50,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 9 SQ. MM. CMOS MICRO-CHIP USING THE IBM CMOS FOUNDRY, Project Title "*Design of a Single-Chip CMOS Integrated Pressure Sensor and Signal Conditioning Circuit*"

2013 FABRICATION SUPPORT (US$50,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 9 SQ. MM. CMOS MICRO-CHIP USING THE IBM CMOS FOUNDRY, Project Title "*Integrated Circuit Design of Bio-cellular Synaptic Transmission Process*"

2013 NZ$ 1,500
TRAVEL SUBSIDY from AUT, Institute for Radio Astronomy And Space Research, to attend Canadian NRC (National Research Council) led Square Kilometer Array (SKA) central signal processor (CSP) DPSG (digital platform study group) Meeting as IC design expert from New Zealand

2013 NZ$ 2,500
Auckland Bio-engineering Institue (ABI), University of Auckland.
Design of Inductive Power Control IC chip

NZ$ 295,000
Ministry of Business, Innovation and Employment (MBIE) sub-contract through AUT.
Project: Design of 8 Terabytes /sec ASIC Correlator chip for Square Kilometer Array (SKA) Survey telescope Central Signal Processor (BIG-DATA Astronomical Signal Processing)

2014 FABRICATION SUPPORT (US$50,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 9 SQ. MM. CMOS MICRO-CHIP USING THE IBM CMOS FOUNDRY, Project Title "*Integrated Circuit Design and implementation of data compression*"

2015 NZ$90,000.00
Callaghan Innovation TIF grant
Project: Micro implantable pressure sensor for lifetime monitoring

2015 FABRICATION SUPPORT (US$50,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 9 SQ. MM. CMOS MICRO-CHIP USING THE IBM CMOS FOUNDRY, Project Title *"Custom High-Performance and Low-Power Sequential-Access Dynamic Memory"*

2016 NZ$ 122,916
Ministry of Business, Innovation and Employment (MBIE) sub-contract extension fund through AUT.
Project: Design of ASIC beamformer chip for Square Kilometer Array (SKA) Central Signal Processor (BIG-DATA Astronomical Signal Processing)

2017 FABRICATION SUPPORT (US$30,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 4 SQ. MM. CMOS MICRO-CHIP USING THE GlOBAL FOUNDRIES CMOS FOUNDRY, Project Title *" Design of a novel low-power burst-mode signal generator chip for telemeter applications"*

NZ$ 25,000
Crown research institution, Plant and Food Research (PFR)
As initial funding for project Title *" Develop a less than 100mg radio transmitter device capable of being detected beyond 100m"*

2018 NZ$ 158,000 (includes 115% overheads)
Ministry of Business, Innovation and Employment (MBIE) sub-contract extension fund through AUT.
Project: Design of ASIC beamformer chip for Square Kilometer Array (SKA) Central Signal Processor (BIG-DATA Astronomical Signal Processing)

NZ$ 35,000
Crown research institution, Plant and Food Research (PFR)
An additional funding for project Title *" Develop a less than 100mg radio transmitter device capable of being detected beyond 100m"*

FABRICATION SUPPORT (US$30,000.00 APPROX)
MOSIS, UNIVERSITY OF SOUTHERN CALIFORNIA, USA
AS FUNDING FOR CHIP FABRICATION COST FOR A 130 NANOMETER 4 SQ. MM. CMOS MICRO-CHIP USING THE GlOBAL FOUNDRIES CMOS FOUNDRY, Project Title *" Novel Millimeterwave Leaky Wave Antenna on Chip with Power Amplifier"*

2019 NZ$ 45,000
Crown research institution, Plant and Food Research (PFR)
As additional funding for project Title, *" Develop a less than 100mg radio transmitter device capable of being detected beyond 100m"*

NZ$10,000
MBIE PreSeed Accelerator Fund through Massey Ventures Ltd.

Project title, “RFID chip fabrication for insect tag”

2020 NZ$ 34,000
Crown research institution, Plant and Food Research (PFR)
As additional funding for project Title, *" Develop a less than 100mg radio transmitter device capable of being detected beyond 100m”*

NZ$ 229,000
Massey university capital equipment round (CER) funding for micro-chip measurement equipment upgrade

Google scholar H-Index: 15, No. of citations: around 900, profile can be found here

RESEARCH COLLABORATIONS (*National and International*):

(1) Development of CMOS MEMS post-processing technique in collaboration with the center for nano-science and engineering at the Indian Institute of Science (IISc), Banglaore, India (2014).
(2) Collaboration with Auckland Bio-engineering Institute (ABI) of University of Auckland on Bio-electronic IC implant design for managing hydrocephalous (2014-2015).
(3) International collaborations with NRC, Canada and CSIRO, Australia on the CSP (Central Signal Processor) MID array and LOW array respectively of the MBIE supported global SKA (Square Kilometer Array) radio-telescope project (2014-2019).
(4) Collaboration on miniaturized inset tag micro-chip design and fabrication with Plant and Food Research, PFR, NZ (2017-todate).

MEMBERSHIP OF PROFESSIONAL ORGANIZATIONS:

SENIOR MEMBER (SM) of IEEE (Institute of Electrical & Electronic Engineers,USA), Member IEEE Solid State Circuits Society and IEEE Circuits and Systems Society

AWARDS AND RECOGNITION:

Co-Winner for 2018 KiwiNet Awards, in the award category:
MinterEllisonRuddWatts Research & Business Partnership Award
for Square Kilometer Array (SKA) Central signal processor design.

Recipient of the *Sharjah Award* in 2002 for outstanding research publication, for the paper entitled, “600 MHz BiCMOS digitally controlled oscillator for clock recovery and frequency synthesis PLLs ," International Journal of Electronics, Taylor and Francis, U.K., vol. 88, no. 5, pp. 529-541, May 2001.

Co-recipient of 2nd position (highly commended award) in 2016 New Zealand Innovation Awards in “Excellence in Research” category for work done in Square Kilometre Array Project.

Co-finalist in 2016 New Zealand Innovation Awards for work done in Square Kilometre Array (SKA) Big Data project in three categories, (1)

Design and Engineering, (2) Technology Solutions, and, (3) Excellence in Research.

Co-finalist (top 10 list) in 2017 Sanitarium New Zealand Innovator of the Year Award.

FEATURED NEWS MEDIA CITATION:

Thursday July 3 2003 ISSUE of GULF NEWS, Dubai, United Arab Emirates, p.2 The nation: Varsity researcher designs 2 GHz silicon chip.

New Zealand Government's PBRF (Performance based research fund) grade and score for the latest (2018) round (published in 2019):

GRADE: A
SCORE: 640/700 with full 7/7 in Research Outputs

LIST OF PUBLICATIONS:

Journal Articles:

185. J83. S. M. Rezaul Hasan, "The "nonideal" drain-loaded source-follower and accurate differential-amplifier analysis," International Journal of Circuit Theory and Applications, Wiley, vol. 48, no. 7, pp.1194-1200, Jul. 2020. (*journal impact factor 1.554*)

184, J82. Ammar Ali and S. M. Rezaul Hasan, "A 38-GHz Millimeter-wave Double-Stacked HBT Class-F-1 High-Gain Power-Amplifier in 130-nm SiGe-BiCMOS," IEEE Transactions On Microwave Theory and Techniques, vol. 68, no. 7, pp. 3039-3044, Jul. 2020. (*Journal impact factor 3.756*)

183, J81. S. M. Rezaul Hasan and Meera Kumari, "A new mid-band analysis methodology for source-followers and drain-loaded source-follower with application in accurate differential-amplifier mismatch analysis," Analog Integrated Circuits and Signal Processing-An International Journal, Springer, vol. 103, pp. 259-271, 2020. (*Journal impact factor 0.8*)

182, J80. Meera Kumari and S. M. Rezaul Hasan, "A New CMOS Implementation for Miniaturized active RFID insect tag and VHF Insect Tracking," IEEE Journal of Radio Frequency Identification, vol. 4, no. 2, pp. 124-136, Jun. 2020.

181, J79. Ibtisam A. Abbas Al-Darkazly and S. M. Rezaul Hasan, "Extra-Low-Frequency Pulse Stimulated Conformational Change in Blood-cell Proteins and Consequent Immune Activity Transformation," IEEE Journal of Translational Engineering in Health and Medicine, available on-line, vol. 8, pp. 1-13, Art no. 4100113, 2020. (*Journal impact factor 2.075*)

180, J78. Meera Kumari and S. M. Rezaul Hasan, “A Low Duty-Cycle Burst-Mode Telemeter Signal Generation Technique for VHF Insect Tracking and Its CMOS Implementation,” IEEE Transactions on Very Large Scale Integration Systems, vol. 28, no. 3, pp. 833-837, Mar. 2020. (*Journal impact factor 1.95*)

179, J77. Meera Kumari, B. K. Bhattacharyya and S. M. Rezaul Hasan, “First Ever Lowest Duty Cycle for Periodic Burst Mode Signals for Insect Telemeter Package Design,” IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 9, no. 10, pp. 2006 -2015, Oct. 2019. (*Journal impact factor 1.86*)

178, J76. Chaoping Zhang and S. M. Rezaul Hasan, “A New Floating-gate Radiation Sensor and Readout Circuit in Standard Single-poly 130nm CMOS Technology,” IEEE Transactions on Nuclear Science, vol. 66, no. 7 (part III, regular papers) pp. 1906 -1915, Jul. 2019. (*Journal impact factor 1.44*)

177, J75. Vignesh Raja Balu and S. M. Rezaul Hasan, “New Optimized ASIC Multiplier in 28nm CMOS for Processing the X-part of FX Correlator in Radio Interferometry,” Experimental Astronomy, Springer, vol. 47, no. 3, pp. 325-343, Jun. 2019. (*Journal impact factor 1.69*)

176, J74. U. Ainuddin, M. Khurram, and S. M. Rezaul Hasan, “Cloning the λ Switch: Digital and Markov Representations,” IEEE Transactions on Nanobioscience, vol. 18, no. 3, pp. 428-436, Jul. 2019. (*Journal impact factor 1.927*)

175, J73. S. M. Rezaul Hasan and Meera Kumari, “Accurate mid-band analysis of the differential-amplifier with active current-mirror load,” IEEE VLSI Circuits and Systems Letter (VCAL), vo. 5, no. 1, Feb. 2019.

174, J72. Chaoping Zhang and S. M. Rezaul Hasan, “A New Floating-Gate MOSFET Model for Analog Circuit Simulation and Design,” Journal of Analog Integrated Circuits and Signal Processing-An International Journal, Springer, vol. 101, no. 1, pp. 1-11, Oct. 2019. (*Journal impact factor 0.8*)

173, J71. V. R. Balu and S. M. Rezaul Hasan, “Computationally Minimized X-part for FX Correlator in Big-data Interferometers,” IEEE Access, vol. 5, pp. 25353-25364, Nov. 2017. (*Journal impact factor 3.557*)

172, J70. M. Waqas, M. Khurram, and S. M. Rezaul Hasan, “Bio-cellular processes modeling on silicon substrate: receptor–ligand binding and Michaelis Menten reaction,” Journal of Analog Integrated Circuits & Signal Processing-An International Journal, Springer, vol. 93, no. 2, pp. 329-340, Nov. 2017. (*Journal impact factor 0.6*).

171, J69. S. M. Rezaul Hasan, “On g_m-boosted follower-amplifier and its novel circuit transformation based mid-band derivations,” Journal of Analog Integrated Circuits & Signal Processing-An International Journal, Springer, vol. 93, no. 1, pp. 107-114, Oct. 2017. (*Journal impact factor 0.8*).

170, J68. Sadia Alam and S. M. Rezaul Hasan, “A Gene-Protein-miRNA Electronic Oscillator,” IEEE Transactions On Circuits and Systems-II: Express Briefs, vol. 64, no. 9, Sep. 2017. (*Journal impact factor 1.66*)

169, J67. Ibtisam A. Abbas Al-Darkazly and S. M. Rezaul Hasan, “Optimized Low-Power CMOS Active-Electrode-pair for Low-Frequency Multi-channel Biomedical Stimulation,” Microelectronics Journal, Elsevier, vol. 66, pp. 18-24, Aug. 2017. (*Journal impact factor 1.322*)

168, J66. Stepan Lapshev and S. M. Rezaul Hasan, “Using Multiple-Accumulator CMACs to Improve Efficiency of the X Part of an Input-Buffered FX Correlator,” Experimental Astronomy, Springer, vol. 43, no. 2, pp. 177-187, Apr. 2017. (*Journal impact factor 2.87*)

167, J65. S. M. Rezaul Hasan, “Novel Inspection-based Mid-band derivations for CMOS Cascodes and gm-Boosted Topologies along-with Simplified Compound Structure Gain-analysis,” Journal of Analog Integrated Circuits & Signal Processing-An International Journal, Springer, vol. 91, no. 1, pp. 21-41, Apr. 2017. (*Journal impact factor 0.8*).

166, J64. Stepan Lapshev and S. M. Rezaul Hasan, “New Low Glitch and Low Power DET Flip-Flops Using Multiple C-Elements,” IEEE Transactions On Circuits and Systems-I: Regular Papers, vol. 63, no. 10, pp. 1673-1681, Oct. 2016 (*Journal impact factor 2.4*)

165, J63. Ibtisam A. Abbas Al-Darkazly and S. M. Rezaul Hasan, “Dual-band Waveform Generator with Ultra-wide Low-frequency Tuning-range,” IEEE Access, vol. 4, pp. 3169-3181, 2016. (*Journal impact factor 3.557*)

164, J62. Ananiah Sundararajan and S. M. Rezaul Hasan, “Quadruply split Cross-driven Doubly Recycled g_m-doubling Recycled Folded Cascode for Micro-Sensor Instrumentation Amplifiers,” IEEE Transactions On Circuits and Systems-II: Express Briefs, vol. 63, no. 6, pp. 543-547, Jun. 2016. (*Journal impact factor 1.66*)

163, J61. Stepan Lapshev and S. M. Rezaul Hasan, “On the architecture for the X part of a very large FX correlator using two-accumulator CMACs,” Experimental Astronomy, Springer, vol. 41, no. 1, pp. 259-270, 2016. (*Journal impact factor 2.0*)

162, J60. Sadia Alam and S. M. Rezaul Hasan, “A VLSI Circuit Emulation of Chemical Synaptic Transmission Dynamics and Post-Synaptic DNA Transcription,” IEEE Transactions on Very Large Scale Integration Systems, vol. 24, no. 2, pp. 678-691, Feb. 2016. *(Journal impact factor 1.698)*

161, J59. Ibtisam A. Abbas Al-Darkazly and S. M. Rezaul Hasan, “A Waveform Generator Circuit for Extra Low Frequency CMOS Micro-Power Applications,” International Journal of Circuit Theory and Applications, Wiley Inter-Science, vol. 44, no. 2, pp. 266-279, Feb. 2016. (*Journal impact factor 1.444*)

160, J58. Ananiah Sundararajan and S. M. Rezaul Hasan, “Elliptic Diaphragm Capacitive Pressure Sensor and Signal Conditioning Circuit Fabricated in SiGe CMOS Integrated MEMS,” IEEE Sensors Journal, vol. 15, no. 3, pp. 1825-1837, Mar. 2015. (*Journal impact factor 2.512*)

159, J57. S. M. Rezaul Hasan, “Simplified Analog CMOS Mid-band Small-signal Analysis utilizing Short-circuits and Incremental Perturbations,” International Journal of Electrical Engineering Education, vol. 52, pp. 356-369, Oct. 2015, Sage publishers, UK.

158, J56. Jie Li and S. M. Rezaul Hasan, “An inductive-degenerated current-bleeding LNA-merged CMOS mixer for 866 MHz RFID reader,” Journal of Analog Integrated Circuits and Signal Processing - An International Journal, Kluwer Academic Publishers (Springer), vol. 80, no. 2, pp. 173-185, 2014. (*Journal impact factor 0.8*).

157, J55. Ananiah Sundararajan and S. M. Rezaul Hasan, “Release Etching and Characterization of MEMS Capacitive Pressure Sensors Integrated on a standard 8-metal 130 nm CMOS process,” Sensors and Actuators ,A: physical, vol. 212, pp. 68-79, Elsevier, 2014. (*Journal impact factor 2.0*)

156. J54. Ananiah Sundararajan and S. M. Rezaul Hasan, “CMOS Integrated Elliptic Diaphragm Capacitive Pressure Sensor in SiGe MEMS,” Microsystem Technologies, Springer, vol. 20, no. 1, pp. 145-155, Jan. 2014. (*Journal impact factor 1*)

155, J53. Ananiah Sundararajan and S. M. Rezaul Hasan, “Post-processing and performance analysis of BEOL integrated MEMS pressure sensor capacitors in 8-metal 130 nm CMOS,” Microelectronic Engineering, vol. 119, pp. 89-94, Elsevier, May 2014. (*Journal impact factor 1.28*)

154, J52. S. Alam, E.M-K Lai, J. Young, S. M. Rezaul Hasan, “Rapid electronic prediction of gene expression regulation in bacterial cells,” Electronics Letters, IET, vol. 50, no. 22, pp. 1566-1568, 2014. (*Journal impact factor 1.0*)

153, J51. Stepan Lapshev and S. M. Rezaul Hasan, “A Low-Power Voltage Limiter/Regulator IC in Standard Thick-Oxide 130 nm CMOS for Inductive Power Transfer Application,” Advances in power electronics, http://dx.doi.org/10.1155/2014/317523, vol. 2014, Article ID 317523, 6 pages, Hindawi Publishing Corporation, 2014.

152, J50. Muhammad Khurram and S. M. Rezaul Hasan, “A Full-Band UWB Common-Gate Band-pass Noise Matched g_m-Boosted series peaked CMOS Differential LNA,” Journal of Analog Integrated Circuits and Signal Processing -An International Journal, Kluwer Academic Publishers (Springer), DOI 10.1007/s10470-013-0085-z, vol. 76, pp. 47-60, 2013. (*Journal impact factor 0.6*).

151, J49. Nabihah Ahmad and Rezaul Hasan, “A 0.8 V 0.23 nW 1.5 ns full-swing pass-transistor XOR gate in 130 nm CMOS,” Active and passive electronic components, vol. 2013, Article ID 148518, 6 pages,

http://dx.doi.org/10.1155/2013/148518, available online, Hindawi Publishing Corporation, 2013. (*Journal impact factor 0.3*)

150, J48. Sadia Alam and S. M. Rezaul Hasan, "'Integrated circuit modeling of bio-cellular post-transcription gene mechanisms regulated by microRNA and proteasome," IEEE Transactions On Circuits and Systems-I: Regular Papers, DOI 10.1109/TCSI.2013.2245451, vol. 60, no. 9, pp. 2298-2310, Sep. 2013. (*Journal impact factor 2.4*)

149, J47. Jack Li and S. M. Rezaul Hasan, "Design and Performance Analysis of a 866 MHz Low-Power Optimized CMOS LNA for UHF RFID," IEEE Transactions On Industrial Electronics, vol. 60, no. 5, pp. 1840-1849, May 2013. (*Journal impact factor 7.168*)

148, J46. N. Ahmad and S. M. Rezaul Hasan, "'Efficient Integrated AES Crypto-Processor Architecture for 8-bit Stream Cipher," Electronics Letters, IET, vol. 48, no. 23, pp. 1456-1457, 2012. (*Journal impact factor 1.15*)

147, J45. S. M. Rezaul Hasan, "A 0.8V 40 Gb/s Novel CMOS Regulated Cascode Trans-impedance Amplifier for Optical Sensing Applications," Journal of Signal Processing Systems, Springer, DOI 10.1007/s11265-012-0707-1, vol. 72, pp. 63-68, 2013. (*Journal impact factor 1.088*)

146, J44. Jack Li and S. M. Rezaul Hasan, "Pulse-Biased Low-Power Low-Phase-Noise UHF LC-QVCO for 866 MHz RFID Front-End," IEEE Transactions On Microwave Theory and Techniques, vol. 60, no. 10, pp. 3120-3125, 2012. (*Journal impact factor 2.897*)

145, J43. Nabihah Ahmad and S. M. Rezaul Hasan, "Low-power Compact Composite Field AES S-Box/Inv S-Box design in 65nm CMOS using Novel XOR Gate," Integration: The VLSI Journal, Elsevier publishers, DOI 10.1016/j.vlsi.2012.06.002, vol. 46, pp. 333-344, 2013. (*Journal impact factor 0.906*)

144, J42. Muhammad Khurram and S. M. Rezaul Hasan, "A Series Peaked Noise Matched gm-Boosted 3.1-10.6 GHz CG CMOS Differential LNA for UWB WiMedia," Electronics Letters, vo.47, no. 24, pp. 1346-1348, IET, Nov. 2011. (*Journal impact factor 1.15*)

143, J41. Sadia Alam and S. M. Rezaul Hasan, "'On the Modeling of Calcium Ion (Ca^{+2}) Conductance in Nerve Membrane Protein Channel as a Memristive Circuit Element," Electronics Letters, vo.47, no. 25, pp. 1361-1363, IET, Dec. 2011. (also features in front-page INSIDE VIEW article, p. 1353 of this issue). (*Journal impact factor 1.15*)

142, J40. Muhammad Khurram and S. M. Rezaul Hasan, "A series peaked gm-boosted 3.1-10.6 GHz CMOS CG UWB LNA for WiMedia," Microwave and Optical Technology Letters, vol. 54, no. 2, pp. 532-535, Wiley Inter-Science, Feb. 2012 (First published online on 15th December, 2011). (*Journal impact factor 0.948*)

141, J39. Robert Fisk and S. M. Rezaul Hasan, “A calibration-free low-cost process-compensated temperature sensor in 130nm CMOS,” IEEE Sensors Journal, vol. 11, no. 12, pp. 3316-3329, Dec. 2011. (*Journal impact factor 2.512*)

140, J38. S. M. Rezaul Hasan and Aanan Khurma, “AC dielectrophoresis using elliptic electrode geometry,” Journal of Sensors, Volume 2011, Article ID 204767, 8 pages, http://dx.doi.org/10.1155/2011/204767, Hindawi Publishing Corporation, 2011. (*Journal impact factor 0.5*)

139, J37. Muhammad Khurram and S. M. Rezaul Hasan, “A 3-5 GHz Current-Reuse g_m-Boosted CG LNA for Ultrawideband in 130nm CMOS,” IEEE Transactions on Very Large Scale Integration Systems, vol. 20, no. 3, pp. 400-409, Mar. 2012. (*Journal impact factor 1.698*)

138, J36. Muhammad Khurram and S. M. Rezaul Hasan, “Novel analysis and optimization of gm-boosted common-gate UWB LNA,” Microelectronics Journal, Vo. 42, no. 2, pp. 253-264, Elsevier publishers, 2011. (*Journal impact factor 1.322*)

137, J35. S. M. Rezaul Hasan, “Transition frequencies and negative resistance of inductively terminated CMOS buffer cell and application in MMW LC VCO,” Active and passive electronic components, vol. 2010, Article ID 542406, 11 pages, http://dx.doi.org/10.1155/2010/542406, Hindawi Publishing Corporation, 2010. (*Journal impact factor 0.3*)

136, J34. Jie Li and S. M. Rezaul Hasan, “A 12dB 0.7V 850uW CMOS LNA for 866 MHz UHF RFID Reader,” Active and passive electronic components, vol. 2010, Article ID 702759, 5 pages, http://dx.doi.org/10.1155/2010/702759, Hindawi Publishing Corporation, 2010. (*Journal impact factor 0.3*)

135, J33. S. M. Rezaul Hasan, “A Novel 0.7V High Sensitivity Complementary Differential MAGFET Sensor for Contactless Mechatronic Applications,” Sensors and Actuators, A: Physical, vol. 163, pp. 138-149, Elsevier publishers, 2010. (*Journal impact factor 2.0*)

134, J32. Muhammad Khurram and S. M. Rezaul Hasan, “A 4mW 3-5 GHz Current Reuse g_m-Boosted Short Channel Common-Gate CMOS UWB LNA ,” Analog integrated circuit and signal processing, Express Letters, Kluwer academic publishers(Springer), vol. 65, pp. 415-418, 2010. (*Journal impact factor 0.6*)

133, J31. Jie Li and S. M. Rezaul Hasan, “A 0.7V 850uW CMOS LNA for UHF RFID Reader,” Microwave and Optical Technology Letters, vol. 52, no. 12, pp. 2780-2782, Wiley Inter-Science, Dec. 2010. (*Journal impact factor 0.6*)

132, J30. Robert Fisk and S. M. Rezaul Hasan, ”Incremental delta-sigma modulators for temperature sensing applications,” International Journal of

Computer Applications in Technology, Inderscience, vol. 39, no. 1/2/3, pp. 66-71, 2010. (*Journal impact factor 0.1*)

131, J29. S. M. Rezaul Hasan, "A Micro-sequenced CMOS Model for Cell Signaling Pathway using G-Protein and Phosphorylation Cascade," International Journal of Computer Applications in Technology, Inderscience, vol. 39, no. 1/2/3, pp. 40-45, 2010. (*Journal impact factor 0.1*)

130, J28. S. M. Rezaul Hasan, "A Digital CMOS Sequential Circuit Model for Bio-Cellular Adaptive Immune Response Pathway Using Phagolysosomic Digestion: A Digital Phagocytosis Engine," International Journal of Biomedical Science and Engineering, vol. 3, no. 5, pp. 470-475, 2010.

129, J27. S. M. Rezaul Hasan, "A Low-Voltage Scalable (1.8V-0.75V) CMOS Folded-Cascode LC Quadrature VCO for RF Receivers," Journal of Circuits, Systems and Computers, vol. 19, no. 4, pp. 835-857, 2010. (*Journal impact factor 0.6*)

128, J26. S. M. Rezaul Hasan, "Analysis and design of a multi-stage CMOS band-pass low-noise pre-amplifier for ultra-wide-band RF receiver," IEEE Transactions on Very Large Scale Integration Systems, vo. 18, no. 4, pp. 638-651, Apr. 2010. (*Journal impact factor 1.698*)

127, J25. S. M. Rezaul Hasan, "A Novel Low-Voltage CMOS Variable Gain Amplifier with Gain-Independent Input Impedance Matching for DTV Tuning Applications," Journal of Circuits, Systems and Computers, vol. 18, no. 6, pp. 1119-1136, Oct. 2009. (*Journal impact factor 0.6*)

126, J24. S. M. Rezaul Hasan and W. L. Xu, "A central pattern generator circuit for rhythmic robotic chewing locomotion in low-voltage analog CMOS technology," Artificial Life and Robotics: An International Journal, Springer-Japan, vol. 14, no. 3, pp. 306-310, Dec. 2009. (*Journal impact factor 0.1*)

125, J23. S. M. Rezaul Hasan, "A Novel Mixed-Signal Integrated Circuit Model for DNA-Protein Regulatory Genetic Circuits and Genetic State Machines, " IEEE Transactions on Circuits and Systems-I: Regular papers, vol. 55, no. 6, pp. 1185-1196, Jun. 2008. (*Journal impact factor 2.4*)

124, J22. S. M. Rezaul Hasan, "An offset compensated sampled-data CMOS comparator circuit for low-power implantable biosensor applications," Journal of Circuits, Systems and Signal Processing, Springer-Verlag, vol. 27, pp. 351-366, Jun. 2008. (*Journal impact factor 0.8*)

123, J21. S. M. Rezaul Hasan and Siti Noorjannah Ibrahim, "Design of an Enhanced Electric Field Sensor Circuit in 0.18μm CMOS for a Lab-on-a-chip Bio-cell Detection Micro-array," Journal of Sensors and Transducers, IFSA, ISSN 1726-5479, vol. 90, pp. 39-47, Apr. 2008.

122, J20. S. M. Rezaul Hasan and Siti Noorjannah Ibrahim, "An Improved CMOS Sensor Circuit using Parasitic Bipolar Junction Transistors for Monitoring the Freshness of Perishables," Journal of Sensors and Transducers, IFSA, ISSN 1726-5479, vol. 90, pp. 276-280, Apr. 2008.

121, J19. S. M. Rezaul Hasan, "Stability Analysis and Novel Compensation of a CMOS Current-feedback Potentiostat Circuit for Electro-chemical Sensors," IEEE Sensors Journal, vol. 7, no. 5, pp. 814-824, May. 2007. (*Journal impact factor 2.5*)

120, J18. S. M. Rezaul Hasan, “A CMOS DCO design using delay programmable differential latches and a novel digital control scheme,” Electrical Engineering, Springer-Verlag, Germany, vol. 89, pp. 569-576, 2007. (*Journal impact factor 0.4*)

119, J17. S. M. Rezaul Hasan and Nazmul Ula, “A Novel Feed-forward Compensation Technique for Single-Stage Fully-Differential CMOS Folded Cascode Rail-to-Rail Amplifier,” Electrical Engineering, Springer-Verlag, Germany, vol. 88, no. 6, pp. 509-517, Aug. 2006. (*Journal impact factor 0.4*)

118, J16. S. M. Rezaul Hasan, “Design of a Low-power 3.5 GHz Broad-Band CMOS Transimpedance Amplifier for Optical Transceivers,” IEEE Transactions on Circuits & Systems I: Regular papers, vol. 52, no. 6, pp. 1061-1072 , 2005. (*Journal impact factor 2.4*)

117, J15. Shahin J. Ashtiani, Omid Shoaei, S. M. Rezaul Hasan, A. M. Jannesari, “On the Parasitic-Sensitivity of Switched-Capacitor Summing-Integrator structures for Σ-Δ Modulators,” IEEE Transactions on Circuits & Systems II: Analog and Digital signal processing, vol. 50, no. 9, pp. 634-640, Sept. 2003. (*Journal impact factor 1.66*)

116, J14. S. M. Rezaul Hasan and Omid Shoaei, “A Fast Macro-Model for Substrate Coupling & Ground Bounce Induced Substrate Noise Simulation in Mixed Signal VLSI,” Journal of Analog Integrated Circuits & Signal Processing-An International Journal, Kluwer academic publishers(Springer), U.S.A., Vol. 37, no. 3, PP. 149-163, Dec. 2003. (*Journal impact factor 0.6*)

115, J13. S. M. Rezaul Hasan and Yufridin Wahab, "Performance enhancement of low-voltage dynamic BiCMOS logic gates by transistor reordering," VLSI Design, An international journal of custom-chip design, simulation and testing, vol. 15, no. 2, pp. 547-553, 2002. (*Journal impact factor 0.2*)

114, J12. S. M. Rezaul Hasan, Lim Chu Aun and Azman Yusof, " 600 MHz BiCMOS digitally controlled oscillator for clock recovery & frequency synthesis PLLs," International Journal of Electronics, Taylor & Francis, U.K., vol. 88, no. 5, pp. 529-541, May 2001. (*Journal impact factor 0.4*)

113, J11. Ho Yoon San and S. M. Rezaul Hasan, "An Architectural Comparison and CMOS Implementation of Sixth-Order Cascaded $\Sigma\Delta$ Modulator," Journal of Analog Integrated Circuits & Signal Processing-An International Journal, Kluwer Academic Publishers(Springer), U.S.A., vol. 26, no. 3, pp. 257-271, March 2001. (*Journal impact factor 0.6*)

112, J10. Jayabalan Kundan and S. M. Rezaul Hasan "Enhanced folded source-coupled logic technique for low-voltage mixed-signal integrated circuits," IEEE Transactions on Circuits & Systems-II: Analog & Digital Signal Processing, vol. 47, no. 8, pp. 810-817, August 2000. (*Journal impact factor 1.66*)

111, J9. S. M. Rezaul Hasan and Yufridin Wahab, "Performance enhancement of low-voltage dynamic BiCMOS logic gates by charge redistribution based transistor reordering," Jurnal Teknikal Pusat Pengajian Electrik dan Elektronik, Vol 4, no. 1 , pp. 1-8, 1998.

110, J8. S. M. Rezaul Hasan and Ho Yoon San "A behavioral simulator for switched-capacitor sigma-delta modulator analog-to-digital converter," ASEAN Journal on Science & Technology for Development, vol. 15, no. 2, pp. 59 - 71 , 1998.

109, J7. S. M. Rezaul Hasan and Chakaravarty Rajagopal " Low Voltage dynamic BiCMOS CLA circuit with carry skip using Novel full-swing logic, " IEEE Journal of Solid State Circuits, vol. 32, no.1, pp. 70 - 78, 1997. (*Journal impact factor 4.181*)

108, J6. S.M. Rezaul Hasan and Ng Kang Siong, " A Parallel Processing VLSI BAM Engine," IEEE Transactions on Neural Networks, vol. 8, no. 2, pp. 424-436,1997. (*Journal impact factor 6.108*)

107, J5. S. M. Rezaul Hasan and Chakaravarty Rajagopal " Improved Low Voltage BiCMOS Dynamic Logic Gates using Output Feedthrough," ASEAN Journal on Science & Technology for Development , vol. 13, no. 2, pp. 87- 92, 1996.

106, J4. S. M. Rezaul Hasan, S.Z. Basri and R. M. Ali, "A VLSI processing element for massively parallel pyramid machine," AMSE Journal On Advances In Modelling & Analysis, A, vol. 31, no. 1, pp. 61- 64, France, 1995.

105, J3. S. M. Rezaul Hasan and Ng Kang Siong, "A VLSI hardware design for bi-directional associative memory neural network," AMSE Journal On Modelling, Measurement & Control, A, vol. 58, no. 1, pp. 11-18, France, 1994.

104, J2. S. M. Rezaul Hasan and C.M. Hadzer, " A new Distributed Arithmetic VLSI Architecture for Discrete Fourier Transform Processor," ASEAN Journal of Science & Technology for Development, vol. 10, no. 2 , pp. 105-114, 1993.

103 J1. S. M. Rezaul Hasan ," A Novel ASIC Architecture for Image Scaling," Jurnal Teknikal Pusat Pengajian Electrik dan Elektronik, vol. 2, no. 1 , pp. 83-90, 1992.

Cover Page Featured Article In Journal:

102, F1. IET ELECTRONICS LETTERS, INSIDE VIEW, The equivalence of nerve membrane protein conductance and memristive circuits has been demonstrated by researchers in New Zealand, Dr. S. M. Rezaul Hasan tells us more, Electronics Letters, 8th December 2011, vol.47, no. 25, p. 1353.

Chapter in Book Series:

101, B2. S. M. Rezaul Hasan and Johan Potgieter, “A centre-of-mass tracker integrated circuit design in nanometric CMOS for Robotic Visual Object Position Tracking,” Studies in Computational Intelligence (SCI), Springer-Verlag, vol. 76, pp. 69-79, 2007.

Book Review:

100, B1. Ali Yeon Md. Shakaff and S. M. Rezaul Hasan, "Microprogrammed Systems Design-A Book review," International Journal of Electrical Engineering Education, Manchester, U.K., 1993.

Conference Proceedings:

99, C99. R. Gallichan, D. McCormick, Rezaul Hasan, P. Hu and D. Budgett, "Analysis of Peak Currents in Integrated Synchronous Rectifiers," Proceedings 13th IEEE International NEWCAS Conference, Grenoble, France, June 7-10, pp. 1-4, DOI:10.1109/NEWCAS.2015.7182040, 2015.

98, C98. Ibtisam A. Abbas Al-Darkazly and S. M. Rezaul Hasan, "A Power Efficient CMOS Cascode Current Mirror to supply independent biasing for Low Voltage Applications," Proceedings 20th Electronics New Zealand Conference, Auckland, New Zealand, pp. 84-88, 2013.

97, C97. Ananiah Durai Sundararajan and S. M. Rezaul Hasan, "Multi - Recycled Folded Cascode Amplifier for Sensor Readout," Proceedings 20th Electronics New Zealand Conference, Auckland, New Zealand, pp. 80-83, 2013.

96, C96. Nabihah Ahmad and S. M. Rezaul Hasan, "Fault Detection Scheme for AES S-box/ Inv S-box," Proceedings 20th Electronics New Zealand Conference, Auckland, New Zealand, pp. 75-79, 2013.

95, C95. Sadia Alam and S. M. Rezaul Hasan, "Bioelectronic Circuit Design for Gene Expression Mechanisms," Proceedings 20th Electronics New Zealand Conference, Auckland, New Zealand, pp. 115-119, 2013. (***Recipient of best electronic design paper award***)

94, C94. Richa Budhiraja, Priya Pundir and S. M. Rezaul Hasan, "A 90nm transimpedance amplifier design for nano-pore based DNA nucleotide sequencer," Proceedings 19th International conference on Mechatronics and machine vision in practice(M2VIP 12), Auckland, pp. 146-149, 2012.

93, C93. Ananiah Sundararajan and S. M. Rezaul Hasan, "A CMOS integrated MEMS capacitive pressure sensor design in a 3D SiGeMEMS process," Proceedings 19th International conference on Mechatronics and machine vision in practice(M2VIP 12), Auckland, pp. 150-155, 2012.

92, C92. Ananiah Sundararajan and S. M. Rezaul Hasan, "A Low Power 4th Order Low Pass Gm-C Filter in 130nm CMOS," Proceedings 18th Electronics New Zealand Conference, Palmerston North, New Zealand, pp. 77-81, 2011.

91, C91. Nabihah Ahmad and S. M. Rezaul Hasan, "Decomposition method for AES Mix Column and Inv Mix Column VLSI architecture optimization," Proceedings 18th Electronics New Zealand Conference, Palmerston North, New Zealand, pp. 91-94, 2011

90, C90. Nabihah Ahmad and Rezaul Hasan, "A new design of XOR-XNOR gates for low power application," Proceedings 2011 IEEE International Conference on Electronic Devices, Systems and Applications (ICEDSA), Kualalumpur, Malaysia, 5 pages, 2011.

89, C89. Jie Li and Rezaul Hasan, "Performance analysis of microstrip line matching network for 866 MHz UHF LNA," Proceedings 17th Electronics New Zealand Conference, Hamilton, New Zealand, pp. 121-128, 2010.

88, C88. Nabihah Ahmad and Rezaul Hasan, “Design of XOR gates in VLSI implementation,” Proceedings 17th Electronics New Zealand Conference, Hamilton, New Zealand, pp. 51-55, 2010.

87, C87. Massoud Alipour and Rezaul Hasan, “Design and simulation of biosensor for DNA detection by CMOS technology,” Proceedings 17th Electronics New Zealand Conference, Hamilton, New Zealand, pp. 63-68, 2010.

86, C86. Nabihah Ahmad, Rezaul Hasan, and Waruszarina Mat Jubadi, “Design of AES S-Box using combinational logic optimization,” Proceedings 2010 IEEE Symposium on Industrial Electronics and Applications, Oct. 3-5, Penang, Malaysia, pp. 679-682, 2010.

85, C85. Robert Fisk and Rezaul Hasan, “Low-cost temperature sensor on a modern sub-micron CMOS process,” Proceedings 16th Electronics New Zealand Conference, Nov. 18-20, Dunedin, New Zealand, pp. 43-48, 2009.

84, C84. Pritesh Lohani and Rezaul Hasan, “Design of an improved fuzzy logic controller micro-chip for washing machine,” Proceedings 16th Electronics New Zealand Conference, Nov. 18-20, Dunedin, New Zealand, pp. 25-30, 2009.

83, C83. Jack Li and Rezaul Hasan, “Comparison of optimized low-power LNA topologies for 866 MHz UHF RFID,” Proceedings 16th Electronics New Zealand Conference, Nov. 18-20, Dunedin, New Zealand, pp. 131-136, 2009.

82, C82. Muhammad Khurram and Rezaul Hasan, “Design of a low-power narrowband amplifier for HF radio applications using CMOS FETs,” Proceedings 16th Electronics New Zealand Conference, Nov. 18-20, Dunedin, New Zealand, pp. 131-136, 2009.

81, C81. Rezaul Hasan, “A digital CMOS sequential circuit model for bio-cellular adaptive immune response pathway using phagolysosomic digestion: A digital phagocytosis engine,” Proceedings 16th Electronics New Zealand Conference, Nov. 18-20, Dunedin, New Zealand, pp. 133-142, 2009.

80, C80. Nazmul Ula and S. M. Rezaul Hasan, “A novel 10GHz CMOS inductive buffered transimpedance amplifier stage for optical transceivers,” Proceedings 2008 IEEE 51st Midwest symposium on circuits and systems, Knoxville, Tennessee, USA, pp. 629-633, 2008.

79, C79. S. M. Rezaul Hasan, ”A Micro-sequenced CMOS Model for Cell Signaling Pathway using G-Protein and Phosphorylation Cascade,” Proceedings 15th International conference on Mechatronics and machine vision in practice(M2VIP), Auckland, pp.57-62, 2008.

78, C78. S. M. Rezaul Hasan, ”A Novel CMOS low-voltage regulated cascode trans-impedance amplifier operating at 0.8V supply voltage,” Proceedings 15th International conference on Mechatronics and machine vision in practice(M2VIP), Auckland, pp.51-56, 2008.

77, C77. Robert Fisk and S. M. Rezaul Hasan, "Incremental delta-sigma modulators for temperature sensing applications," Proceedings 15th International conference on Mechatronics and machine vision in practice(M2VIP), Auckland, pp.63-67, 2008.

76, C76. S. M. Rezaul Hasan, "An inductive buffered trans-impedance amplifier stage for optical transceivers in 130nm CMOS," Proceedings 2008 IEEE 20th International Conference of Microelectronics (ICM 2008), Sharjah, UAE, pp. 219-222, Dec. 2008.

75, C75. Muhammad Khurram and Rezaul Hasan, "Design of a sub-gigahertz complementary cascode LNA with active input matching," Proceedings 15th Electronics New Zealand Conference, Nov. 24-25, Auckland, New Zealand, pp. 39-44, 2008.

74, C74. Muhammad Khurram and Rezaul Hasan, "Design of a full-band gm-boosted current reused UWB LNA," Proceedings 15th Electronics New Zealand Conference, Nov. 24-25, Auckland, New Zealand, pp. 25-28, 2008.

73, C73. Rezaul Hasan and Muhammad Khurram, "A new CMOS negative resistance oscillator buffer-cell with a fundamental f-trans limit," Proceedings 15th Electronics New Zealand Conference, Nov. 24-25, Auckland, New Zealand, pp. 29-32, 2008.

72, C72. S. M. Rezaul Hasan and Nazmul Ula, "Analog CMOS Charge Model for Molecular Redox Electron-Transfer Reactions and Bio-Chemical Pathways," Proceedings 2008 IEEE International Conference on Circuits and Systems (ISCAS 2008), pp. 2038-2041, Seattle, Washington.

71, C71. S. M. Rezaul Hasan, W. L. Xu and Nazmul Ula, "Low-voltage analog current-mode central pattern generator circuit for robotic chewing locomotion using 130nm CMOS technology," Proceedings 2007 IEEE 19th International Conference of Microelectronics (ICM 2007), Cairo, Egypt, pp. 167-171, Dec. 2007.

70, C70. S. M. Rezaul Hasan and Siti Noorjannah Ibrahim, "An enhanced CMOS electric field sensor circuit for cells sensing lab-on-a-chip application," Proceedings International conference on sensing technology(ICST), Palmerston North , pp. 255-259, Nov. 2007.

69, C69. S. M. Rezaul Hasan and Siti Noorjannah Ibrahim, "An improved MOS sensor circuit for emulating the quantum of freshness in perishables using parasitic bipolar devices," Proceedings International conference on sensing technology(ICST), Palmerston North , pp. 260-264, Nov. 2007.

68, C68. S. M. Rezaul Hasan and Jie Li, "A bias-controlled noise-cancelling CMOS tuned low noise amplifier for UWB transceivers," Proceedings IEEE ICECS, Morocco , pp. 1205-1208, Dec. 2007.

67, C67. S. M. Rezaul Hasan, “A CMOS RF variable gain amplifier with gain-independent input impedance matching,” Proceedings 14th Electronics New Zealand Conference, Nov. 12-13, Wellington, New Zealand, pp. 53-58, 2007.

66, C66. S. M. Rezaul Hasan and W. L. Xu, “Low-voltage analog CMOS central pattern generator circuit for rhythmic robotic chewing locomotion,” Proceedings 14th Electronics New Zealand Conference, Nov. 12-13, Wellington, New Zealand, pp. 297-301, 2007.

65, C65. S. M. Rezaul Hasan, “A PMOS-diode differential body-driven offset compensated 0.5V sampled-data comparator for biosensor applications,” Proceedings 20th IEEE International conference on VLSI Design (VLSID’07), Bangalore, INDIA, pp. 913-918, Jan. 2007

64, C64. S. M. Rezaul Hasan and Johan Potgieter, “A novel CMOS sampled-data center of mass tracker circuit for robotic visual feedback object tracking,” Proceedings the 3rd International conference on Autonomous Robots and agents, Dec. 12-14, Palmerston North, New Zealand, pp. 213-218, 2006.

63, C63. Robert Fisk and S. M. Rezaul Hasan, “Analysis of Internally-Generated Noise in Bandgap References,” Proceedings 13th Electronics New Zealand Conference, Nov. 13-14, Christchurch, New Zealand, pp. 18-23, 2006.

62, C62. S. M. Rezaul Hasan, “ A Novel Body-driven Deep nanometric CMOS Operational Transconductance Buffer for Implantable Bio-electronics,” Proceedings 13th Electronics New Zealand Conference, Nov. 13-14, Christchurch, New Zealand, pp. 163-166, 2006.

61, C61. S. M. Rezaul Hasan, “A Novel Offset compensated CMOS Sub-1V Sampled-data Comparator for Biosensor Applications,” Proceedings 13th Electronics New Zealand Conference, Nov. 13-14, Christchurch, New Zealand, pp. 75-80, 2006.

60, C60. S. M. Rezaul Hasan, “A Novel 16-bit CMOS Digitally Controlled Oscillator,“ Proceeedings IEEE ASIA-PACIFIC conference on Circuits & Systems, Dec. 5-7, Singapore, pp. 527-530, 2006.

59, C59. S. M. Rezaul Hasan and Nazmul Ula, “A Novel Current Feed-back Sub-Nano-Siemen Transconductance Circuit Suitable for Large Time-Constant Bio-medical Applications,“ Proceeedings IEEE ASIA-PACIFIC conference on Circuits & Systems, Dec. 5-7, Singapore, pp. 687-690, 2006.

58, C58. S. M. Rezaul Hasan, “Stability and compensation technique for a CMOS amperometric potentiostat circuit for redox sensors,” Proceedings IEEE ASIA-PACIFIC Conference on Circuits & Systems, Dec. 5-7, Singapore, pp. 878-881, 2006.

57, C57. S. M. Rezaul Hasan and Nazmul Ula, “A Novel Current-feedback Nano-Siemen Transconductance Circuit Suitable for Large Time-constant

Applications, " Proceedings IEEE Midwest conference on Circuits & Systems, Puerto Rico, pp. 557-560, 2006.

56, C56. S. M. Rezaul Hasan and Nazmul Ula, "An Inductive-bounce Enhanced Output-pad for CMOS UltraWideBand RF Applications, " Proceedings IEEE Midwest conference on Circuits & Systems, Puerto Rico, pp. 358-361, 2006.

55, C55. S. M. Rezaul Hasan and Nazmul Ula, "A 16-bit CMOS digitally controlled oscillator using a novel control scheme, " Proceedings IEEE Midwest conference on Circuits & Systems, Puerto Rico, pp. 680-684, 2006.

54, C54. S. M. Rezaul Hasan, "A CMOS Low Noise Pre-Amplifier for Ultra-Wide-Band RF Receiver," Proceedings IFIP VLSI System-on-Chip 2005 Conference, Perth, Australia, pp. 545-549, 2005.

53, C53. S. M. Rezaul Hasan, "A Novel Wide-Swing Wide-Bandwidth Scalable Low-Voltage Analog CMOS Multiplier for Communication Signal Processing," Proceedings 12th Electronics New Zealand Conference, Nov 14-15, Manukau, New Zealand, pp. 31-34, 2005.

52, C52. S. M. Rezaul Hasan, "A novel integrated circuit model for mRNA transcription in bio-cellular processes," Proceedings 12th Electronics New Zealand Conference, Nov 14-15, Manukau, New Zealand, pp.7-12, 2005.

51, C51. S. M. Rezaul Hasan, "A fifth order LC butterworth tuned CMOS low noise pre-amplifier for ultrawideband RF receiver," Proceedings 12th Electronics New Zealand Conference, Nov 14-15, Manukau, New Zealand, pp.25-29, 2005.

50, C50. A. Luxton and S. M. Rezaul Hasan, "A low power high gain CMOS folded cascade amplifier," Proceedings 12th Electronics New Zealand Conference, Nov 14-15, Manukau, New Zealand, pp. 47-50, 2005.

49, C49. S. M. Rezaul Hasan, "A novel CMOS integrated circuit model for cellular DNA-protein regulatory mRNA transcription process," Proceedings 12th International conference on biomedical engineering, Dec 7-10, Singapore, IFMBE CD proceedings, ISBN: 981054572x, 2005.

48, C48. S. M. Rezaul Hasan and Nazmul Ula, "A Capacitor-free Feed-forward Compensated Single-stage Merged Topology Fully-differential CMOS Folded Cascode Amplifier ," Proceedings 3rd IEEE North East Workshop on Circuits and Systems, Quebec City, Canada, pp.179-182, 2005.

47, C47. S. M. Rezaul Hasan, "A High Efficiency 3GHz 24-dBm CMOS Linear Power Amplifier for RF Application," Proceedings 5th IEEE workshop on Systems-on-chip for Real-time applications, July 19-21, Alberta, Canada, IEEE Computer Society Press, pp. 503-507, 2005.

46, C46. S. M. Rezaul Hasan, "A transmission-gate CMOS folded LC quadrature VCO for low-power RF transceivers", Proceedings 11th Electronics New Zealand Conference, Nov 15-16, Palmerston North, New Zealand, pp.171-175, 2004.

45, C45. A. M. Jannesari, S. M. Rezaul Hasan, and Mehrdad Sharif-Bakhtiar, "Design of wide-band opamp with improved DC-gain for high-Q high frequency

switched-capacitor filters", Proceedings 11th Electronics New Zealand Conference, Nov 15-16, Palmerston North, New Zealand, pp.77-81, 2004.

44, C44. S. M. Rezaul Hasan and Nazmul Ula, "A 4GHz Low-Power Folded-Cascode CMOS LC Quadrature VCO for RF Transceivers", Proceedings The 2004 International Conference on VLSI (VLSI'04), June 21-24, Las Vegas, Nevada, pp.339-342, 2004.

43, C43. S. M. Rezaul Hasan, "A scalable low-voltage extended swing CMOS LC quadrature VCO for RF Transceivers", Proceedings 4th IEEE workshop on Systems-on-chip for Real-time applications, July 19-21, Alberta, Canada, IEEE Computer Society Press, pp.131-135, 2004.

42, C42. Nazmul Ula and S. M. Rezaul Hasan, "Simulation and Optimization of a Wide-Bandwidth Transimpedance Amplifier", Proceedings of the Twelfth IASTED International Conference on Applied Simulation and Modelling, Marbella, Spain, September 3-5, pp 136 - 140, 2003.

41, C41. S. M. Rezaul Hasan and Maamar Bettayeb, "An Order RecursivePipelined Real-Time VLSI HOS Engine for System-On-Chip Implementation," Proceedings, IEEE TENCON, vol. 4, pp. 1257-1261, Bangalore, India, Oct. 2003.

40, C40. S. M. Rezaul Hasan, "A 5GHz CMOS Voltage-Current Feedback Wide-band Transimpedance Amplifier for Optical Transceivers," IEEE ICECS, pp. 567-570 , Sharjah, Dec. 2003.

39, C39. S. M. Rezaul Hasan, "A 5GHz CMOS digitally controlled oscillator with a 3GHz tuning range for PLL applications," IEEE ICECS 2003, pp. 208-211, Sharjah, Dec. 2003

38, C38. S. M. Rezaul Hasan, "A 5GHz CMOS broad-band transimpedance amplifier for optical transceivers," Proceedings, IEEE GCC Industrial Electrical & Electronic Engineering Conference, Bahrain, May 13-14, 2003.

37, C37. S. M. Rezaul Hasan, "A high performance wide-band CMOS transimpedance amplifier for optical transceivers," Proceedings 3rd IEEE workshop on Systems-on-chip for Real-time applications, Calgary, Canada, IEEE Computer Society Press, pp. 82-85, 2003

36, C36. S. M. Rezaul Hasan, " An Inductively Peaked 3.5GHz Broad-band CMOS Trans-impedance Amplifier for Optical Transceivers," CD Proceedings GSPx International Signal Processing Conference, Dallas, Texas, USA, March 31 - April 3, paper no: 431, 2003.

35, C35. S. M. Rezaul Hasan and Yufridin Wahab, " Reduction of power dissipation in dynamic BiCMOS logic gates by transistor reordering," Proceedings International Symposium on Integrated Circuits, Devices & Systems, pp. 117-121, September, 2001.

34, C34. S. M. R. Hasan and N. A. Quadir, “A 2.5 GHz Current-Feedback Transimpedance Amplifier for Optical Transceivers”, IEEE Region 10 Conference, Singapore, August 2001

33, C33. S. M. R. Hasan, “Effect of globalization on electrical and computer engineering education”, Forum: The changing role of engineering education in the information age – innovation and tradition, Sharjah, Society of Engineers, pp. 50, UAE, April 2001

32, C32. S. M. R. Hasan and S. Kumar, “Design of a high speed and high-performance CMOS serial bus data transceiver,” SPIE Proceedings, Design, Modeling, & Simulation in Microelectronics, pp. 352-357, Volume 4228, 2000

31, C31. S. M. R. Hasan and N. A. Quadir, “High performance transimpedance amplifier for OC-48 Optical transceiver application,” SPIE Proceedings, Design, Modeling, & Simulation in Microelectronics, pp. 342-351, Volume 4228, 2000

30, C30. Ho Yoon Sun and S. M. Rezaul Hasan " A sixth-order 2-1-1-2 cascaded CMOS sigma-delta modulator," Proc. 8 th International Conference on IC Design, Technology & Manufacture (ISIC '99), pp. 286-289, Singapore , 1999.

29, C29. Lim Chu Aun and S. M. Rezaul Hasan " A BiCMOS implementation of an all digital phase lock loop for VLSI communication applications," Proc. 8 th International Conference on IC Design, Technology & Manufacture (ISIC '99), pp. 290-292, Singapore , 1999.

28, C28. Lim Chu Aun and S. M. Rezaul Hasan, "An all Digital BiCMOS Phase Lock Loop for VLSI Processors, " GLSVLSI-99, IEEE Computer Society, USA, pp. 318-320, 1999 .

27, C27. S. M. Rezaul Hasan and Yufridin Wahab, "Performance enhancement of low-voltage dynamic BiCMOS logic gates by charge redistribution based transistor reordering," Proc. International conference on computing & information technology (ICCIT), Dhaka, Dec. 1998.

26, C26. Ho Yoon San, S. M. Rezaul Hasan and Nazmul Ula, "CMOS Implementation of a Sixth-Order Cascaded Sigma-Delta Modulator Architecture," Proc. 42 nd IEEE Midwest symposium on Circuits & Systems, USA, 1999.

25, C25. Azman Yusof, Lim Chu Aun and S. M. Rezaul Hasan, "600 MHz digitally controlled BiCMOS oscillator (DCO) for VLSI signal processing and communication applications," GLSVLSI-98, IEEE Computer Society, USA, pp. 71-76, 1998.

24, C24. Ho Yoon San and S. M. Rezaul Hasan., “A sixth-order CMOS sigma-delta modulator,“ Proceedings Eleventh Annual IEEE International ASIC Conference, pp. 63 –66, 13-16 Sep. 1998.

23, C23. Ho Yoon Sun and S. M. Rezaul Hasan "A simulation tool for switched-capacitor sigma-delta converter," Proc. 7 th International

Conference on IC Design, Technology & Manufacture (ISIC '97), pp. 216-219, Singapore , 1997.

22, C22. Ho Yoon Sun and S. M. Rezaul Hasan " A behavioral simulator for switched-capacitor sigma-delta modulator analog-to-digital converter," Proc. IASTED International Conference on Modelling, Simulation and Optimization , pp. 311-314, Singapore , 1997.

21, C21. K. Jayabalan and S. M. Rezaul Hasan "Current mode BiCMOS Folded source-coupled logic circuits, " IEEE International Conference on Circuits & Systems (ISCAS), pp. 1880-1883, Hong Kong , 1997.

20, C20. K. Jayabalan and S. M. Rezaul Hasan "Improved current-mode BiCMOS logic circuit technique," Proc. ROVPIA'96 Conference, pp. 586-592, Ipoh, Malaysia 1996.

19, C19. S. M. Rezaul Hasan and Chen Seong Chin "A new VLSI architecture for multi layer perceptron(MLP) network," Proc. IEEE TENCON Conference, pp. 352-354, Perth, Australia , 1996.

18, C18. S. M. Rezaul Hasan and Ho Yoon Sun, "Low power, high performance switched-capacitor second order sigma-delta modulator suitable for battery operated signal processing applications," Proc. IEEE TENCON Conference, pp. 728-730, Perth, Australia , 1996.

17, C17. S.M. Rezaul Hasan and Ho Yoon Sun " Low power, high performance switched-capacitor second order sigma-delta modulator suitable for battery operated signal processing applications," Proc. GlobalTRONICS Electronics Design Conference, Suntec city, Singapore, 1996 .

16, C16. S. M. Rezaul Hasan, Chakaravarty Rajagopal and Nazmul Ula " Improved Low Voltage Dynamic BiCMOS Logic Gates using Output Feedthrough," Proceedings 1996 IEEE 39 th Midwest Symposium on Circuits & Systems, pp. 94-97, Ames, Iowa, USA .

15, C15. C. M. Hadzer, S. M. Rezaul Hasan and Lau Kwee Sing, " Improved Singular Value Decomposition by using Neural Networks," Proc. IEEE International Conference on Neural Networks (ICNN '95), vol. 1, pp. 438 - 442, Perth, Australia, 1995.

14, C14. S. M. Rezaul Hasan and Ng Kang Siong , "A VLSI BAM Neural Network Chip for Pattern Recognition Applications," Proc.. IEEE International Conference on Neural Networks (ICNN '95), vol. 1, pp 164 - 168, Perth, Australia, 1995.

13, C13. Norlaili Mohd. Noh & S. M. Rezaul Hasan, "VLSI Viterbi Decoder for deep space communications," Proceedings 2nd IEEE Malaysia International Conference on Communications, pp. 14.6.1 - 14.6.4, Langkawi, Malaysia, 1995.

12, C12. Norlaili Mohd. Noh and S. M. Rezaul Hasan, "Single Chip VLSI implementation of a systolic array viterbi decoder," Proceedings 7th

International Conference on Microelectronics(ICM'95), pp. 63-66, Kualalumpur, Malaysia, 1995.

11, C11. S. M. Rezaul Hasan and Chakaravarty Rajagopal , "Novel 1.5V BiCMOS dynamic logic gates using output feedthrough," Proceedings 7th International Conference on Microelectronics(ICM '95), pp. 67-69, Kualalumpur, Malaysia, 1995.

10, C10. S.M. Rezaul Hasan, "Design of a pH controller ASIC Fuzzy logic chip for industrial application," Proc. GlobalTRONICS Electronics Design Conference, WTC, Singapore, 1994 .

9, C9. S. M. Rezaul Hasan and Norlaili bte Mhd. Noh, " Application of FPGA Device in the Design of a Systolic Array Viterbi Decoder," Proc. Fifth International Conference on Signal Processing Applications & Technology (ICSPAT), pp. 1459-1464, Dallas, Texas, USA, 1994.

8, C8. S. M. Rezaul Hasan and Ng Kang Siong , "A VLSI BAM Neural Network Chip for Pattern Recognition Applications," Proc. Australian Microelectronics Conference (MICRO '93), Brisbane, Australia, 1993.

7, C7. S. M. Rezaul Hasan, " A new Distributed -pipeline VLSI Distributed Arithmetic Architecture for Discrete Fourier Transform Processor," Proc. AL-AZHAR Engineering Third International Conference, Nasr City, Cairo, Egypt, 1993.

6, C6. S.M. Rezaul Hasan, G. N. Kumer, R. S. Fager," A Bi-level Weighted ASIC Neural Processor Slice," Proc. International Micro-electronics & Systems Conference , PWTC, Kuala Lumpur,Malaysia, 1993.

5, C5. S. M. Rezaul Hasan and Ng Kang Siong, " VLSI BAM CHIP," Proc. International Conference on Signal Processing Applications & Technology (ICSPAT), pp. 1637-1640, Santa Clara, California, USA, 1993.

4, C4. S. M. Rezaul Hasan , "A Novel Pipeline LSI Architecture for Image Magnification and Reduction," Proc. IEEE Asian Electronics Conference, Hong kong, 1987.

3, C3. S. M. Rezaul Hasan, "A Novel LSI Architecture for Image Scaling," Proc. IEEE TENCON Conference, pp. 110-114, Seoul, Korea, 1987.

2, C2. John Wu, Han Jen, S. M. Rezaul Hasan, " VLSI Processor Design using Standard-cell and Custom-cell Methodology," Proc. 2nd International Symposium on IC Design and Manufacture(ISIC-87), pp. 137-160, Singapore, 1987.

1, C1. S. M. Rezaul Hasan , " A new VLSI Architecture for Image Data rate Discrete Cosine Transform Processor," Proc. IASTED International Symposium on Signal Processing and its Applications, pp. 750-755, Brisbane, Australia, 1987.

Thesis, Dissertation & Reports:

1. S.M. Rezaul Hasan , "Distributed VLSI Image Processors and Master Quad-slice Transformers" , Ph.D. Dissertation, School of Engineering & Applied Science, University of California, Los Angeles, USA, 1985.

2. S. M. Rezaul Hasan and Zulkifli Hj. Abdul Kadir Bakti, "A Pipe-line Multiplier MPR Chip", Report Mesyuarat "Asean Subcommittee on Micro-electronics and Information Technology" ke 8, 24-26 Jun, 1993, Manila, Filipina.

3. Co-author for "SKA1-Survey Physical Implementation Proposal Feasibility White Paper," Auckland, New Zealand, May, 2013.

SEMINARS:

16th Oct. 2010 UNIVERSITY OF CANTERBURY, CHRISTCHURCH, DEPARTMENT OF MECHANICAL ENGINEERING
Topic: *CMOS in Micro-mechatronics and Micro-robotics (along with Prof. Gurvinder Virk)*

20th Sept. 2012 EICS Seminar at Massey University, entitled "*Design of low-power Trans-impedance amplifier*"

12th April, 2013 SKA Meeting, MBIE, NZ GOVERNMENT, Wellington
Topic: *Massey University Background And Participation In SKA Work Packages*

12th Feb., 2015 Computing for SKA colloquium 2015, entitled “ASIC design for SKA – SKASIC”

9th Feb., 2017 Computing for SKA colloquium 2017, entitled “The importance of analog/analog VLSI in the world of digital and Big-data”

15th Feb., 2018 Computing for SKA colloquium 2018, entitled “Multiplier-free FPGA LUT implementation of Radio-astronomical signal processing using distributed arithmetic and Massey science spinoffs in SKA related PhD projects”

EXPERIENCE IN JOURNAL EDITORSHIP:

1. Editor, International Journal of Circuit Theory and Applications (Wiley) (2020-)
2. Editor of Journal of active and passive electronic components (2010 – present).

EXPERIENCE IN PAPER REVIEW:

Perform review of a large number of journal and conference papers annually including mostly IEEE journals and conferences.

POST-GRADUATE SUPERVISIONS/POST-GRADUATE COMPLETIONS AS MAIN (CHIEF) SUPERVISOR IN ELECTRONICS ENGINEERING AT MASSEY:

10 Ph.D. completions and 4 Masters completions in Massey University as Main (Chief) Supervisor.
Ph.D. supervisions as Main (Chief) Supervisor:

(1) Robert Fisk: Analog and Mixed Signal IC Design for sensors.(*Completed, 2009*)

(2) Jack Li: CMOS Radio Frequency IC Design for RFID. (*Completed, 2011*)

(3) Muhammad Khurram: CMOS Radio Frequency Integrated Circuit Design for Ultrawideband.(*Completed, 2012)*

(4) Mahsa Mohaghegh: Machine Translation from English to Persian. (*Completed, 2013*)

(5) Nabihah Ahmad: Compact CMOS VLSI implementation of Advanced Encryption Algorithm in 65nm CMOS.(*Completed, 2014*)

(6) Ananiah Sunderarajan: Analog CMOS integrated MEMS pressure sensor.(*Completed*, *2015*)
(7) Sadia Alam: Analog CMOS VLSI modelling of nanobiosystems. (*Completed*, *2015*)

(8) Ibtisham Abbas: Design of very low frequency synthesizer for bio applications. (*Completed*, 2017)

(9) Stepan Lapshev: Design of very high speed Correlator chip for survey radio telescope. (BIG DATA, SKA project) (*Competed,* 2018)

(10) Vignesh Raja Balu: A Novel Mixed-signal CMOS 6Gbps VLSI Array processing element. (BIG DATA, SKA project) (Completed, 2020 – awaiting oral exam)

(11) Meera Kumari: Investigation, design and fabrication OF miniaturized novel CMOS active RFID tags. (*in progress*)

(12) Ammar Ali: Novel Millimeterwave Integrated Circuit Front End with Steerable On-Chip Antenna. (*in progress*)

(13) Naina Singhal: Novel circuit design for CMOS Analog Beamformer chip (*in progress*)

(14) Elamana Marakkadath Dalin: A CMOS Integrated Energy Harvesting (renewable energy) Solution for Application Specific IC's (*in progress*)

EXTERNAL EXAMINER OF DOCTORAL THESIS:

Examined 11 doctoral thesis from Anna University, India, (2006-2012), 4 from NIT, India (2014-2020), 2 doctoral thesis from Nanyang Technological University, Singapore (2011), 1 doctoral thesis from Multi-media University, Malaysia (2013), and, 1 Master and 2 PhD from University of Auckland (2017-2018).

EXPERIENCE IN CONFERENCE ORGANIZATION:

Program Committee member:
International conference on IC Design (ISIC), 1987 Singapore
International conference on Robotics, Vision and Parallel processing, 1999, Ipoh, Malaysia
International conference on electronics, computers and systems (ICECS), 2003, Sharjah, UAE
International conference in mechatronics, and machine vision in practice (M2VIP), 2008, Auckland.

International conference in mechatronics, and machine vision in practice (M2VIP), 2012, Auckland.
24th IEEE International conference on Electronics, Circuits and Systems (IEEE ICECS 2017)
25th IEEE International conference on Electronics, Circuits and Systems (IEEE ICECS 2018)
2018 International Conference on Analog VLSI Circuits, Chiang Mai, Thailand (AVIC 2018)
26th IEEE International conference on Electronics, Circuits and Systems (IEEE ICECS 2019)

Program co-ordinator:
Electronics New Zealand Conference (2013), Auckland.

EXPERIENCE AS CONFERENCE SESSION CHAIR:
Many conferences world-wide

CONTRIBUTION TO SOCIETY:

(1) Participation in Massey University Open Day (2006 – 2016)
(2) Participation in Albany Engineering and Food Technology Degree Show (2010-2016)
(3) Supervision of overseas internship students from India (2009, 2011) and Australia (2011)
(4) Provided Practical Training in electronics to undergraduate students through the Center for Research in Analog and VLSI design during Summer 2014-2016
(5) Provide support through IEEE mentoring program

REFEREES

AVAILABLE ON REQUEST

Ph.D. Advisors at UCLA:
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